PVP 12

Code: EC4T2, EM4T1, EE4T6

II B.Tech - II Semester – Regular Examinations - JUNE 2015

PULSE & DIGITAL CIRCUITS
(Common for ECE, ECM, EEE)

Duration: 3 hours Marks: 5x14=70

Answer any FIVE questions. All questions carry equal marks

1. a) Define Rise time. Derive the expression for rise time. Also give the relationship between Rise time and bandwidth. 7 M

b) i) A symmetrical periodic square waveform with peak amplitude of 'V' volts, and time period of 'T' is applied to an RC integrator circuit as an input. Find the steady state voltage across each element in the circuit.

ii) An ideal 1μs pulse is applied to an RC circuit. Calculate and plot the output waveform when the upper 3 dB frequency is 10 MHz and 0.1 MHz. 7 M

2. a) With neat sketch, explain the working of a Two level diode clipping circuit and draw the transfer characteristics of it. 7 M

b) State and prove clamping circuit theorem. 7 M

3. a) Explain, with reference to a semiconductor diode, the terms: storage time, transitions time and reverse recovery time. 7 M

b) Explain the design of transistor as a switch. 7 M

4. a) A fixed bias binary uses NPN silicon transistors with worst case values of $V_{cc}=V_{BB}=6V$, R1=4.7kΩ, R2=27kΩ, Rc=1.2kΩ, $V_{ce}(sat)=0.5V$, $V_{be}(sat)=1V$, ICBO=10nA, V_{be} cutoff=0V. Find hfe(min) and verify that when one transistor is OFF, the other is ON. Find the stable state voltages and Currents. 7 M

b) Define Hysteresis Voltage. Explain, what are the steps to involve elimination of hysteresis loop in Schmitt trigger circuit with neat sketch. 7 M

5. a) With neat sketch, explain the working of a Monostable Multi and derive the expression for delay width of monostable multi. 7 M

b) Design a collector coupled Astable multivibrator for the following specifications: f=10KHz, Vcc=9V, Ic(max)=20mA and hfe=20. 7 M

6. a) Explain deviation from linearity in voltage time base (sweep) generator. Derive the errors present in it and give the relationship between them. 7 M

b) Draw the circuit of a bootstrap sweep circuit and explain its operation. Derive the expression for Sweep error 'es'. 7 M

7. a) Explain the principle of synchronization to a sweep circuit (UJT) with the help of necessary waveforms and also give the conditions to achieve synchronization. 7 M

b) With the help of a block diagram explain the concept of frequency division without Phase delay and phase jitter. 7 M

8. a) Draw and explain an emitter coupled bidirectional sampling gate. 7 M

b) Explain the operation of a four diode sampling gate with a neat circuit. 7 M